T89C51CC01 PROGRAMMING SPECIFICATION

Doc Control

Revision	Pages	Purpose of Modifications	Originator	Date
A	all	Creation	T. Lysé	10/10/00
B	6-7 7-8-9-10	Modification Erase and Programming sequences Modification of the Read sequence : Width of P2.7 pulse	T. Lysé	29/11/00
C	3-4-5-6-7	Modification Erase sequence : Add PGPL and BPGPL test modes	T. Lysé	03/01/01
D	3-6-12	Suppression of PGXC mode and add SSB byte in Extra Row Area	T. Lysé	20/04/01

1. FLASH/EEPROM Parallel Programming

1.1. Signature bytes

Four hardware read only registers have to be accessed with parallel static test modes (mode TMS) in order to control the FLASH parallel programmimg:

- Manufacturer code
- Device ID # 1: Family code
- Device ID # 2: Memories size and type
- Device ID # 3: Name and revision

As these registers can only be accessed by hardware, they must be read by the parallel programmers and then copied in the XAF in order to make their values accessible by software (ISP or API).

1.2. Set-up modes

In order to program and verify the FLASH areas : FM0 (User Memory), the FM1 (Boot+Data Memory) and Extra Row Area or to read the signature bytes, the T89C51CC01 is placed in specific set-up modes (See Figure 1).

Control and program signals must be held at the levels indicated in Table 1.and Table 2.(Please notice that each mode is defined over the two tables

Mode Name	Mode	Rst	Psen	Ale	EA	P2.6	P2.7	P3.6	P3.7	P0[7..0]
PELCK	Program or Erase Lock. Disable the Erasure or Programming access	1	0	_ _ |_|	1	1	0	1	0	xx
PEULCK	Program or Erase UnLock. Enable the Erasure or Programming access	1	0	Note 3	1	1	0	1	0	55-AA
PGML	User Memory Page Load (up to 128 bytes)	1	0	Note 2	1	0	1	0	1	Din
PGMC	User Memory Write Page Always precedeed by PGML	1	0	2x10ms (Note 4)	1	0	1	1	1	xx
PGMV	User Memory Read Code Data (byte)	1	0	1	1	0	_ _ |_|	1	1	Dout
VSB	Read Hardware Byte (=HSB) (Fuse+Lock Bits)	1	0	1	1	0	_ _ |_|	0	1	Dout (Note 5)
PGLSB	Load Hardware Byte (=HSB) (Fuse+Lock Bits)	1	0	Note 2	1	1	1	0	0	Din (Note 5)
PGCSB	Write Hardware Byte (=HSB) (Fuse+Lock Bits)	1	0	10 ms	1	1	1	0	1	xx
PGPL	Test Page Load (Note 7)	1	0	Note 2	1	0	0	1	0	Din
CERR	Chip Erase User + XAF + Lock Bits	1	0	10ms	1	1	0	0	0	xx
PGXC	Write Page Extra Memory (XAF) Always precedeed by PGML	1	0	2x10ms (Note 4)	1	1	1	0	1	xx
RXAF	Read Extra Memory (XAF)	1	0	1	1	0	_ _ |_|	0	0	Dout
TMS	Read Signature bytes 30h (Manufacturer code) 31h (Device ID #1) 60h (Device ID #2) 61h (Device ID #3)	1	0	1	1	0	_ _ |_|	0	0	Dout = 58h D7h F7h FFh
BDPGML	Boot + Data Memories Page Load (up to 128 bytes)	1	0	Note 2	1	0	1	0	1	Din
BPGMC	Boot Memory Write Page Always precedeed by BDPGML	1	0	2x10ms	1	0	1	1	1	xx
DPGMC	Data Memory Write Page Always precedeed by BDPGML	1	0	2x10ms (Note 4)	1	0	1	1	1	xx
BPGMV	Boot Memory Read Code Data (byte)	1	0	1	1	0	_ _ |_|	1	1	Dout
DPGMV	Data Memory Read Code Data (byte)	1	0	1	1	0	_ _ |_|	1	1	Dout
BDPGPL	Boot + Data Memory Test Page Load (Note 7)	1	0	Note 2	1	0	0	1	0	Din
BDCERR	Chip Erase Boot + Data Memories	1	0	10ms	1	1	0	0	0	xx

Table 1. T89C51CC01 Set-up modes Definition (1)

Mode Name	Mode	P1[7..0]	P2[5..0]	P3.0	P3.1	P3.2	P3.3	P3.4	P3.5
PELCK	Program or Erase Lock. Disable the Erasure or Programming access	xx	xx	x	x	x	1	x	x
PEULCK	Program or Erase UnLock. Enable the Erasure or Programming access	xx	xx	x	x	x	0	x	x
PGML	Memory Page Load (up to 128 bytes)	A0-A7	A8-A13	1 (Note 6)	x	x	0	A14	x
PGMC	Write Page Always precedeed by PGML	A0-A7	A8-A13	1 (Note 6)	x	Note 1	0	A14	x
PGMV	Read Code Data (byte)	A0-A7	A8-A13	1 (Note 6)	x	x	1	A14	x
VSB	Read Hardware Byte (=HSB)	xx	xx	1	x	x	1	x	x
PGLSB	Load Hardware Byte (=HSB) (Fuse+Lock Bits)	xx	xx	1	x	x	0	x	x
PGCSB	Write Hardware Byte (=HSB) (Fuse+Lock Bits)	xx	xx	1 (Note 6)	x	Note 1	1	x	x
PGPL	Test Page Load (Note 7)	xx	xx	1	x	x	0	x	x
CERR	Chip Erase User + XAF + Lock Bits	xx	xx	1 (Note 6)	x	x	0	x	x
PGXC	Write Page Extra Memory (XAF) Always precedeed by PGML	A0-A7 (0-7F)	xx	1 (Note 6)	x	Note 1	0	x	x
RXAF	Read Extra Memory (XAF)	Addr A0-A7 (0-7F)	xx	1 (Note 6)	x	x	0	x	x
TMS	Read Signature bytes 30h (Manufacturer code) 31h (Device ID #1) 60h (Device ID #2) 61h (Device ID #3)	30h 31h 60h 61h	x	x	x	x	1	x	x
BDPGML	Boot + Data Memory Page Load (up to 128 bytes)	A0-A7	A8-A10	0 (Note 6)	x	x	0	x	x
BPGMC	Boot Memory Write Page Always precedeed by PGML	A0-A7	A8-A10	0 (Note 6)	x	Note 1	0	x	0
DPGMC	Data Memory Write Page Always precedeed by PGML	A0-A7	A8-A10	0 (Note 6)	x	Note 1	0	x	1
BPGMV	Boot Memory Read Code Data (byte)	A0-A7	A8-A10	0 (Note 6)	x	x	1	x	0
DPGMV	Data Memory Read Code Data (byte)	A0-A7	A8-A10	0 (Note 6)	x	x	1	x	1
BDPGPL	Boot + Data Memory Test Page Load (Note 7)	xx	xx	0 (Note 6)	x	x	0	x	x
BDCERR	Chip Erase Boot + Data Memories	xx	xx	0 (Note 6)	x	x	0	x	x

Table 2. T89C51CC01 Set-up modes Definition (2)

***Note 1**: P3.2 is pulled low during programming to indicate RDY/BUSY.*
(P3.2 = 1 Ready; P3.2 = 0 Busy).
***Note 2**: In Page Load Mode the current byte is loaded on ALE rising edge.*
***Note 3**: After a power up all external test mode to program or to erase the FLASH are locked to avoid any untimely programming or erasure. After each programming or erasure test mode, it's advised to lock this feature (test mode PELCK).*
To validate the test mode mode PEULCK the following sequence has to be applied:
Test Mode PEULCK with ALE = 1.
Pulse on ALE (min width=25clk) with P0=55 (P0 latched on ALE rising edge)
Pulse on ALE (min width=25clk) with P0=AA (P0 latched on ALE rising edge)
***Note 4**: Use of externally timed mode of the memory block. 2 pulses are needed for all modes but PGCSB and CERR : one erase pulse + one program pulse. The width of each are independent.*
***Note 5**: D[0-3] = SB[0-3], D[4-7] = FB[0-3]. SB means Security Bit or Lock Bit. FB means Fuse Bit. See hardware byte definition.*
***Note 6**: P3.0 enables selection of FM0 if set to 1 and selection of FM1 if set to 0.*
***Note 7**: PGPL and BDPGPL modes load the same byte in all the 128 bytes latches. before erasing the area..*

1.3. Definition of terms

Address Lines:P1.0-P1.7, P2.0-P2.5, P3.4, respectively for A0-A14.

Data Lines:P0.0-P0.7 for D0-D7

Control Signals:RST, $\overline{PSEN}$, P2.6, P2.7, P3.2, P3.3, P3.6, P3.7.

Program Signals: ALE/$\overline{PROG}$, $\overline{EA}$

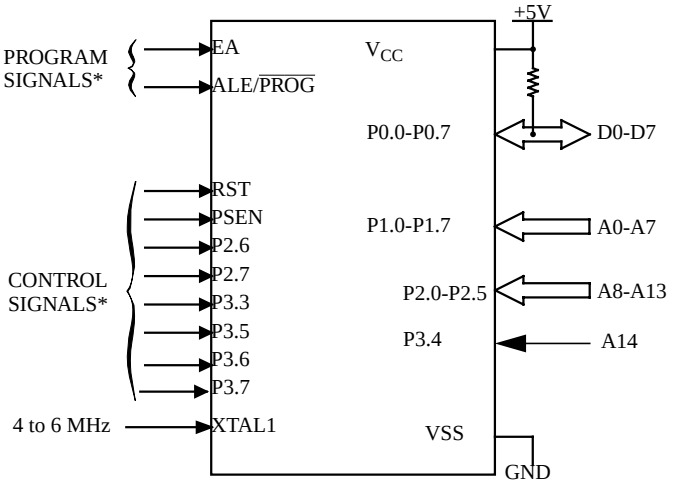

Figure 1. Set-Up Modes Configuration

1.4. Programming Algorithm

To program the T89C51CC01 the following sequence must be exercised:

- Check the signature bytes (TMS mode)
- Check the Hardware Byte (=HSB) (VSB mode)
- Store the Hardware Byte value : HSBSaved.

If the security bits are activated, the following commands must be done before programming:

- Unlock test modes (PEULCK mode, pulse 55h and AAh)
- Test Page Load with data equal to FFh (PGPL mode)
- Chip erase (CERR mode)
- Write (HSBSaved OR $\overline{\text{HSBBitsReserved}}$) in the HSB, where the "HSBBitsReserved" byte value is 0x38h. Reserved bits must keep their previous values.

  Load data in latch (PGLSB mode)

  Write data (PGCSB mode)
- Write the signature bytes content in the XAF[1] :

  Load data in latch (PGML mode)

  Write data (PGXC mode)
- Disable programming access (PELCK mode)

To write a page in the FLASH User memory (FM0), execute the following steps:

- Step 0: Enable programming access (PEULCK mode)
- Step 1 : Set the address counter to the first address of the page.
- Step 2: Activate the combination of control signals (PGML mode)
- Step 3: Input the valid address of the address counter on the address lines (High order bits of the address must be stable during the complete ALE low time).
- Step 4: Input the appropriate data on the data lines.
- Step 5: Pulse ALE/$\overline{\text{PROG}}$ once.
- Step 6 : Increment the address counter.

Repeat step 3 through 6 changing the address and data for end of a 128 bytes page

- Step 7: Activate the combination of control signals (PGMC mode)[2]
- Step 9: Pulse ALE/$\overline{\text{PROG}}$ twice until the specified write time is reached. (1 pulse for erase and 1 pulse for write, even if Chip Erase has been performed before)

Repeat step 2 through 9 changing the address and data until the entire array or until the end of the object file is reached (See Figure 2.)

- Step 10: Disable programming access (PELCK mode)

To write a page in the FLASH Boot memory (FM1), the sequence is similar except the use of BDPGML mode instead of PGML mode and BPGMC mode instead of PGMC mode.

1. As the boot loader and the XAF content is lost after a "chip erase", it must be reprogrammed if needed. Boot Status Byte (BSB), Software Boot Vector (SBV) and Software Security Byte must be also reprogrammed.
2. **Keep the latest address of the current page on the address lines**

To write a page in the FLASH Data memory (FM1), the sequence is similar except the use of BDPGML mode instead of PGML mode and DPGMC mode instead of PGMC mode.

To erase Data memory (FM1) and Boot Memory (FM1), the sequence is similar as the user memory erase sequence except the use of BDPGPL mode instead of PGPL mode and BCERR mode instead of CERR mode.

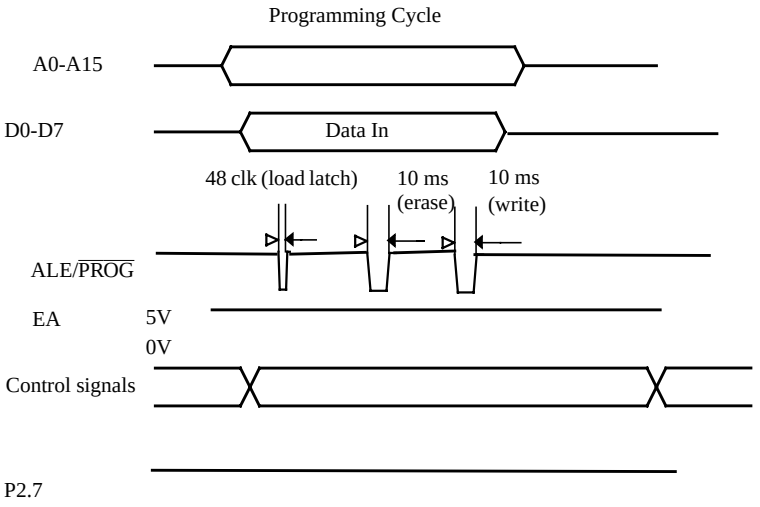

Figure 2. Programming Signal's Waveform

1.5. Verify algorithm

Verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the T89C51CC01.

P 2.7 is used to enable data output.

To verify the T89C51CC01 code the following sequence must be exercised:

- Step 1:Activate the combination of program and control signals (PGMV)
- Step 2: Input the valid address on the address lines.
- Step 3: Pulse P2.7, read data on the data lines on the rising edge of the pulse. This pulse must start 48 Xtal clocks after addresses are present on the address lines and pulse width 12 Xtal Clock minimum.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 3.).

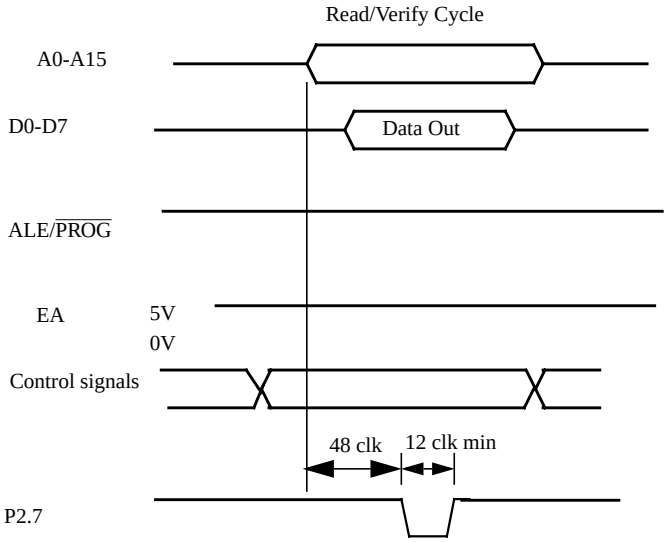

Figure 3. Verification Signal's Waveform

1.6. Read Extra Row Area algorithm

Read XAF must be done to know values of Boot Status Byte and Boot Vector Address in a view to display these information for modification by the user.

P 2.7 is used to enable data output.

To read XAF the T89C51CC01 code the following sequence must be exercised:

- Step 1:Activate the combination of program and control signals (RXAF mode)
- Step 2: Input the valid address on the address lines (A0-A7).
- Step 3: Pulse P2.7, read data on the data lines on the rising edge of the pulse. This pulse must start 48 Xtal clocks after addresses are present on the address lines and pulse width 12 Xtal Clock minimum.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 4).

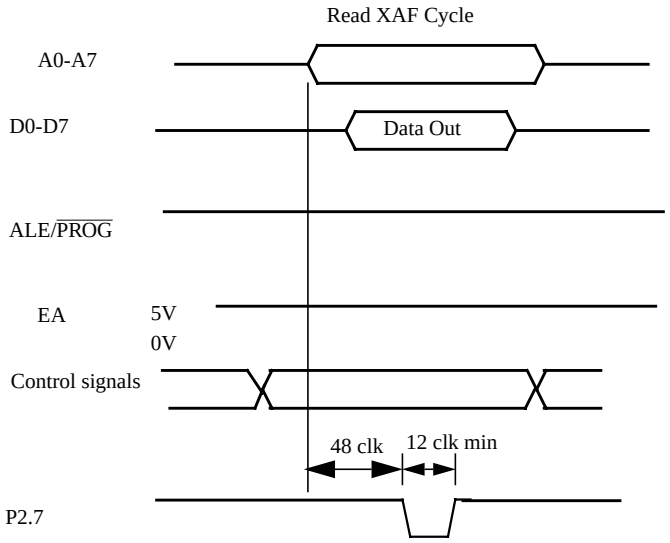

Figure 4. Read Extra Row Area Signal's Waveform

1.7. Write Extra Row Area algorithm

Write Extra Row Area must be done after a chip erase to copy signature bytes. This is also necessary for modifying the Boot Status Byte, Boot Vector Address and Extra Byte.

To ¨program XAF of the T89C51CC01 the following sequence must be exercised:

- Input the valid address on the address lines (High order bits of the address must be stable during the complete ALE low time)
- Activate the combination of control signals (PGML mode)
- Input the appropriate data on the data lines.
- Pulse ALE/$\overline{\text{PROG}}$ once.
- Activate the combination of control signals (PGXC mode)
- Step 9: Pulse ALE/$\overline{\text{PROG}}$ twice until P3.2 is high or the specified write time is reached. (See Figure 5)

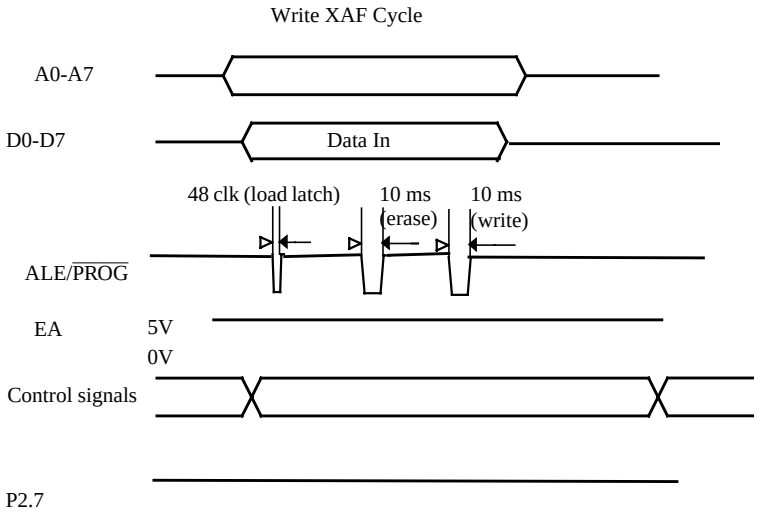

Figure 5. Write Extra Row Area Signal's Waveform

1.8. Read signature bytes algorithm

To read the signature bytes of the T89C51CC01, the following sequence must be exercised:

- Step 1:Activate the combination of program and control signals (TMS)
- Step 2: Input the valid address of the signature bytes (on the address lines.
- Step 3: Pulse P2.7, read data on the data lines on the rising edge of the pulse. This pulse must start 48 Xtal clocks after addresses are present on the address lines and pulse width 12 Xtal Clock minimum.

Repeat step 2 through 3 changing the address for the others signature bytes (See Figure 6).

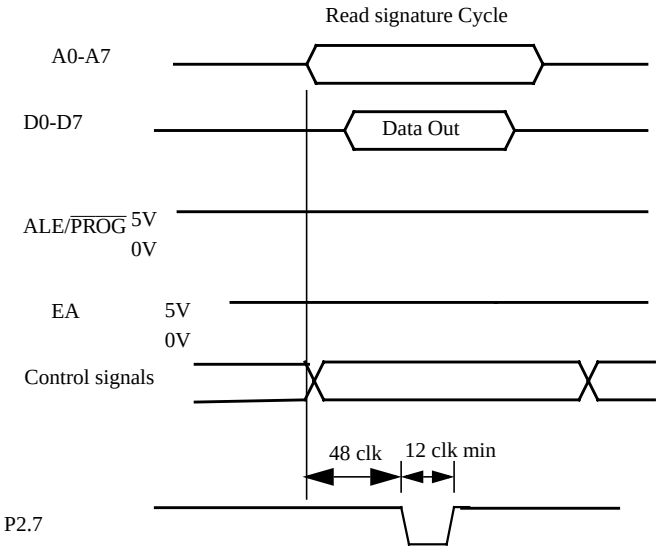

Figure 6. Read Signature Bytes Signal's Waveform

1.9. Write Hardware Byte

7	6	5	4	3	2	1	0
X2B	**BLJB**	**-**	**-**	**-**	**LB2**	**LB1**	**LB0**

Bit Number	Bit Mnemonic	Description
7	X2B	**X2 Bit** Set this bit to start in standard mode Clear this bit to start in X2 mode.
6	BLJB	**Boot Status Bit** Set this bit to start the user's application on next RESET (@0000h) located in FM0, Clear this bit to start the boot loader(@F800h) located in FM1.
5-3	-	**Reserved** The value read from these bits are indeterminate.
2-0	LB2:0	**Lock Bits**

Table 3. Hardware Byte

Default value after erasing chip: 11xxx111b

NOTE:
Only the 4 MSB bits can be access by software.
The 4 LSB bits can only be access by parallel mode.
The reserved bits must keep their previous value.

To program the T89C51CC01 hardware byte, the following sequence must be exercised:

- Check the Hardware Byte (=HSB) (VSB mode)
- Store the HSB value : HSBSaved.
- Write the Hardware Byte :

  ((HSB user defined value) AND ($\overline{\text{HSBBitsReserved}}$)) OR ((HSBSaved AND (HSBBitsReserved)))

  where the "HSBBitsReserved" byte value is 0x38h.
- Load data in latch (PGLSB mode)
- Write data (PGCSB mode)

See Figure 2. for the programming signal's waveforms.

1.10. Extra memory mapping

The memory mapping the T89C51CC01 software registers in the Extra FLASH memory is described in the table below.

Table 4. Extra Row Memory Mapping (XAF)

	Address	Default content
Copy of device ID #3	0061h	FFh
Copy of device ID #2	0060h	F7h
Copy of device ID #1	0031h	D7h
Copy of Manufacturer Code: ATMEL	0030h	58h
Extra Byte	0006h	FFh
Software Security Byte	0005h	FFh
Copy of HSB (level 4 by default)	0004h	18h
Software Boot Vector	0001h	F8h
Boot Status Byte	0000h	FFh

All other addresses are reserved