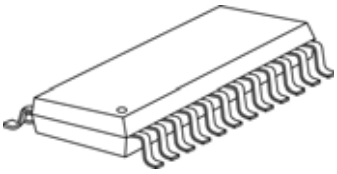
16-Channel PWM Constant Current LED Driver For Time-multiplexing Applications

Features

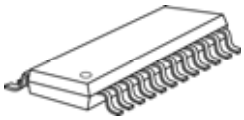
- 3V-5.5V supply voltage
- Constant output current range: 3~45mA
  - 3~45mA @ 5V supply voltage
  - 3~30mA @ 3.3V supply voltage
- Backward compatible with MBI5026 and MBI5030 in package
- 16 constant current output channels
- Built-in 4K-bit SRAM to support time-multiplexing for 1 ~ 8 scans
- 16-bit /14-bit color depth PWM control
- Scan-type Scrambled-PWM technology to improve visual refresh rate
- 6-bit programmable output current gain
- Excellent output current accuracy:
  Between channels: <±1.5% (typ.), and
  Between ICs: <±3% (typ.),
- Staggered delay of output to reduce EMI
- Maximum data clock frequency: 30MHz
- Schmitt trigger input

Small Outline Package



GF: SOP24L-236-1.00

Shrink SOP



GP: SSOP24L-150-0.64

Product Description

MBI5050 is designed for LED video applications using internal Pulse Width Modulation (PWM) control with selectable 16-bit / 14-bit color depth. MBI5050 features a 16-bit shift register which converts serial input data into each pixel's gray scale of the output port. Sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs with a wide range of V_F variations. The output current can be preset through an external resistor. Moreover, the preset current of MBI5050 can be further programmed to 64-step for LED global brightness adjustment.

The innovative architecture with embedded SRAM is designed to support up to 8:1 time-multiplexing applications. User only needs to send the whole frame data once and to store in the embedded SRAM of the LED driver, instead of sending every time when the scan line is changed. It helps save the data bandwidth and achieve high grayscale with very low data clock rate.

With scan-type Scrambled-PWM (S-PWM) technology, MBI5050 enhances Pulse Width Modulation by scrambling the "on" time of each scan line into several "on" periods and sequentially drives each scan line for a short "on" period. The enhancement equivalently increases the visual refresh rate of scan-type LED displays. MBI5050 drives the corresponding LEDs to the brightness specified by image data. With MBI5050, all output channels can be built with 16-bit color depth (65,536 gray scales). Each LED's brightness can be calibrated enough from minimum to maximum brightness with compensated gamma correction or LED deviation information inside the 16-bit image data. When building a 16-bit color depth video, S-PWM technology reduces the flickers and improves the image fidelity. Also, MBI5050 offloads the signal timing generation of the host controller which just needs to feed data into drivers.

Floor 6-4, No.18, Pu-Ting Rd., Hsinchu, Taiwan 30077, ROC.
TEL: +886-3-579-0068, FAX: +886-3-579-7534 E-mail: info@mblock.com.tw

Block Diagram

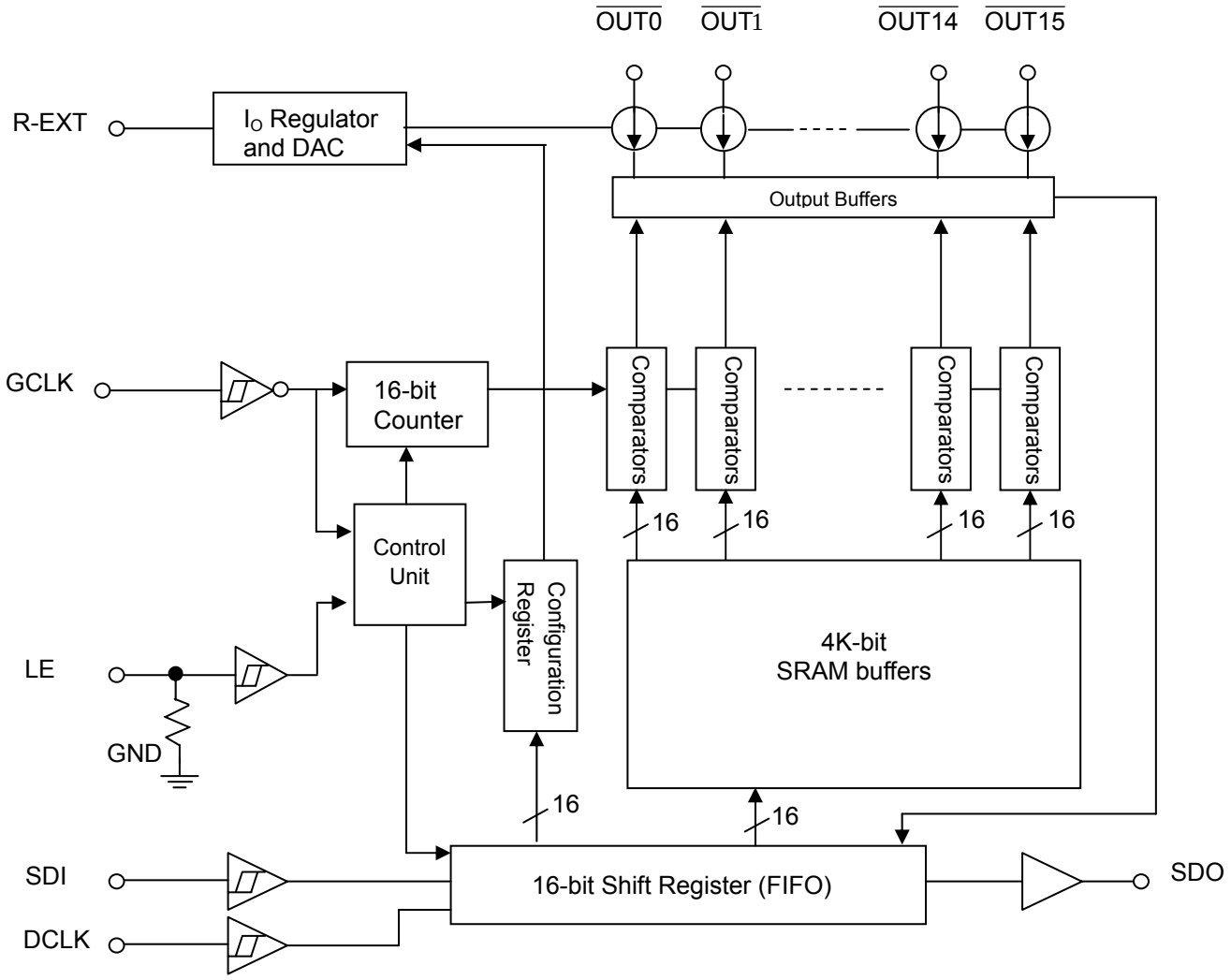
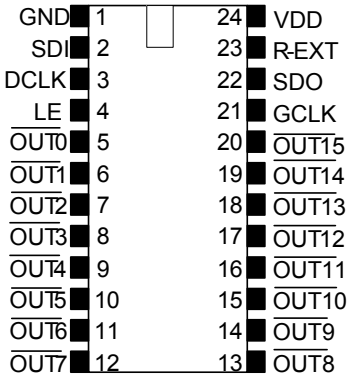


Figure 1

Pin Configuration



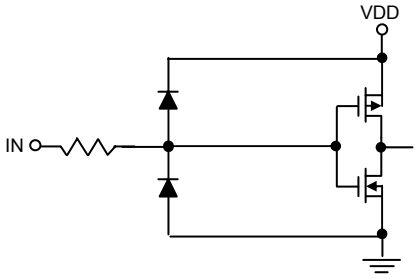
MBI5050 GF/GP

Terminal Description

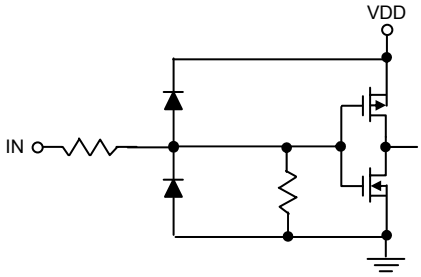
Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
DCLK	Clock input terminal used to shift data on rising edge and carries command information when LE is asserted.
LE	Data strobe terminal and controlling command with DCLK
$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminals
GCLK	Gray scale clock terminal Clock input for gray scale. The gray scale display is counted by gray scale clock comparing with input data.
SDO	Serial-data output to the receiver-end SDI of next LED driver
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

Equivalent Circuits of Inputs and Outputs

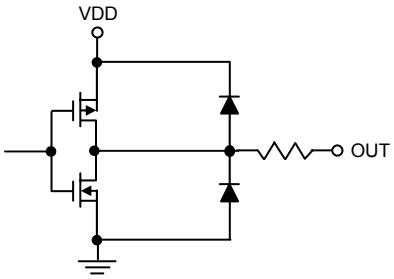
GCLK, DCLK, SDI terminal



LE Terminal



SDO Terminal



Maximum Rating

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~7	V
Input Pin Voltage (SDI)		V_{IN}	-0.4~V_{DD}+0.4	V
Sustaining Voltage at OUT Port		V_{DS}	-0.5~17	V
Output Current		I_{OUT}	+45	mA
GND Terminal Current		I_{GND}	720	mA
Power Dissipation	GF Type	P_D	1.87	W
(On 4 Layer PCB, Ta=25°C)*	GP Type		1.79	
Thermal Resistance	GF Type	$R_{th(j-a)}$	66.69	°C/W
(On 4 Layer PCB, Ta=25°C)*	GP Type		69.5	
Junction Temperature		$T_{j,max}$	150**	°C
Operating Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. User should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested operation temperature of the device is under 125°C.

Electrical Characteristics(V_{DD}=5.0V, Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		3	-	45	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	μA
Output Voltage	SDO	V_{OH}	I_{OH}=-1.0mA		4.6	-	-	V
		V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
Current Skew (Channel)		dI_{OUT}	I_{OUT}=25mA V_{DS}=1.0V	R_{ext}=560Ω	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=25mA V_{DS}=1.0V	R_{ext}=560Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation*		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V, R_{ext}=560Ω@25mA		-	±0.1	±0.5	% / V
Output Current vs. Supply Voltage Regulation*		$\%/dV_{DD}$	V_{DD} within 4.5V and 5.5V		-	±1.0	±2.0	% / V
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	"Off" (SDI=DCLK=GCLK =0Hz)	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	3.4	6.0	mA
		I_{DD}(off) 2	R_{ext}=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	7.7	12	
		I_{DD}(off) 3	R_{ext}=360Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	9.7	15	
	"On" (SDI=10MHz, DCLK=GCLK=20MHz)	I_{DD}(on) 1	R_{ext}=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	7.8	15	
		I_{DD}(on) 2	R_{ext}=360Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	9.8	20	

*One channel on.

Electrical Characteristics (V_{DD}=3.3V, Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		3	-	30	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	µA
Output Voltage	SDO	V_{OH}	I_{OH}=-1.0mA		2.9	-	-	V
		V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
Current Skew (Channel)		dI_{OUT}	I_{OUT}=25mA V_{DS}=1.0V	R_{ext}=560Ω	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=25mA V_{DS}=1.0V	R_{ext}=560Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V, R_{ext}=560Ω@25mA		-	±0.1	±0.5	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 3.0V and 3.6V		-	±1.0	±2.0	% / V
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	"Off" (SDI=DCLK=GCLK =0Hz)	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	3.2	6	mA
		I_{DD}(off) 2	R_{ext}=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	7.4	12	
		I_{DD}(off) 3	R_{ext}=360Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	9.4	15	
	"On" (SDI=10MHz, DCLK=GCLK=20MHz)	I_{DD}(on) 1	R_{ext}=560Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	7.4	15	
		I_{DD}(on) 2	R_{ext}=360Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	9.4	20	

*One channel on.

Test Circuit for Electrical Characteristics

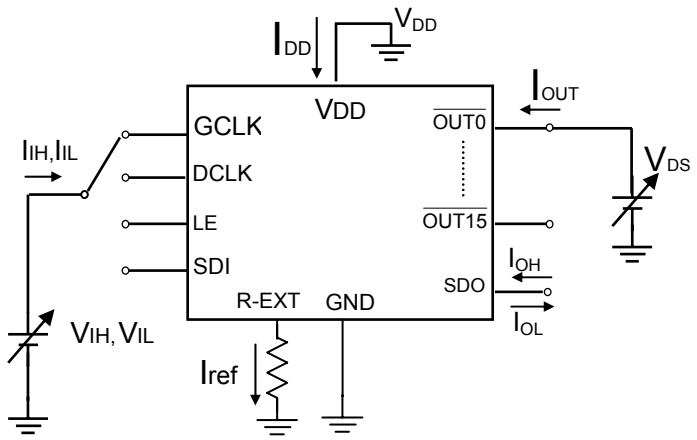


Figure 2

Switching Characteristics(V_{DD}=5.0V)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK↑	t_{SU0}	$V_{IH}=V_{DD}$ V_{IL}=GND R_{ext}=680Ω V_{LED}=4.0V V_{DS}=1V R_L=150Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF	5	-	-	ns
	LE – DCLK↑	t_{SU1}		8	-	-	ns
	LE ↓ (Vsync)* – GCLK	t_{SU2}		7	-	-	ns
Hold Time	DCLK↑ - SDI	t_{H0}		6	-	-	ns
	DCLK↑ - LE	t_{H1}		8	-	-	ns
	GCLK – LE ↓ (Vsync)*	t_{H2}		7	-	-	ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	25	33	ns
	GCLK – $\overline{OUT4n}$ **	t_{PD1}		-	35	-	ns
Staggered Delay of Output	$\overline{OUT4n+1}$ ***	t_{DL1}		-	5	-	ns
	$\overline{OUT4n+2}$ ***	t_{DL2}		-	10	-	ns
	$\overline{OUT4n+3}$ ***	t_{DL3}		-	15	-	ns
Data Clock Frequency		F_{DCLK}		-	-	30	MHz
Gray Scale Clock Frequency****		F_{GCLK}		-	-	33	MHz
Min. Clock(GCLK or DCLK) Pulse Width		$t_{W(CLK)}$		10	-	-	ns
Ratio of (GCLK freq)/(DCLK freq)		$R_{(GCLK/DCLK)}$		20	-	-	%
Output Rise Time of Output Ports		t_{OR}		-	15	25	ns
Output Fall Time of Output Ports		t_{OF}		-	15	25	ns

* Vsync refers to “Vertical Sync” command. More details can be referred to P12.

**Output waveforms have good uniformity among channels.

***Refer to the Timing Waveform, where n=0, 1, 2, 3.

****With uniform output current.

Switching Characteristics (V_{DD}=3.3V)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK↑	t_{SU0}	$V_{IH}=V_{DD}$ V_{IL}=GND R_{ext}=680Ω V_{LED}=4.0V V_{DS}=1V R_L=150Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF	7	-	-	ns
	LE – DCLK↑	t_{SU1}		10	-	-	ns
	LE ↓ (Vsync)* – GCLK	t_{SU2}		10	-	-	ns
Hold Time	DCLK↑ - SDI	t_{H0}		8	-	-	ns
	DCLK↑ - LE	t_{H1}		10	-	-	ns
	GCLK – LE ↓ (Vsync)*	t_{H2}		10	-	-	ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	30	40	ns
	GCLK – $\overline{OUT4n}$ **	t_{PD1}		-	45	-	ns
Staggered Delay of Output	$\overline{OUT4n+1}$ ***	t_{DL1}		-	5	-	ns
	$\overline{OUT4n+2}$ ***	t_{DL2}		-	10	-	ns
	$\overline{OUT4n+3}$ ***	t_{DL3}		-	15	-	ns
Data Clock Frequency		F_{DCLK}		-	-	25	MHz
Gray Scale Clock Frequency****		F_{GCLK}		-	-	20	MHz
Min. Clock(GCLK or DCLK) Pulse Width		$t_{W(CLK)}$		12	-	-	ns
Ratio of (GCLK freq)/(DCLK freq)		$R_{(GCLK/DCLK)}$		20	-	-	%
Output Rise Time of Output Ports		t_{OR}		-	25	35	ns
Output Fall Time of Output Ports		t_{OF}		-	25	35	ns

* Vsync refers to “Vertical Sync” command. More details can be referred to P12.

**Output waveforms have good uniformity among channels.

***Refer to the Timing Waveform, where n=0, 1, 2, 3.

****With uniform output current.

Test Circuit for Switching Characteristics

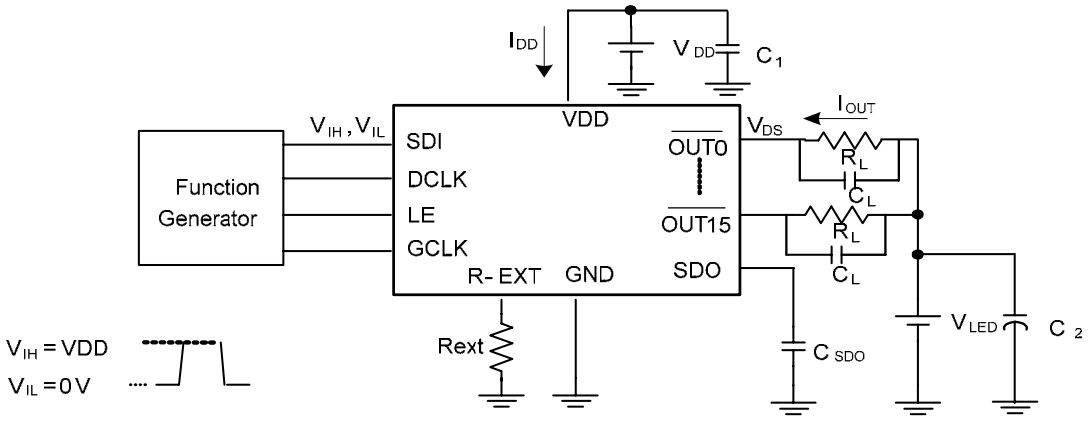
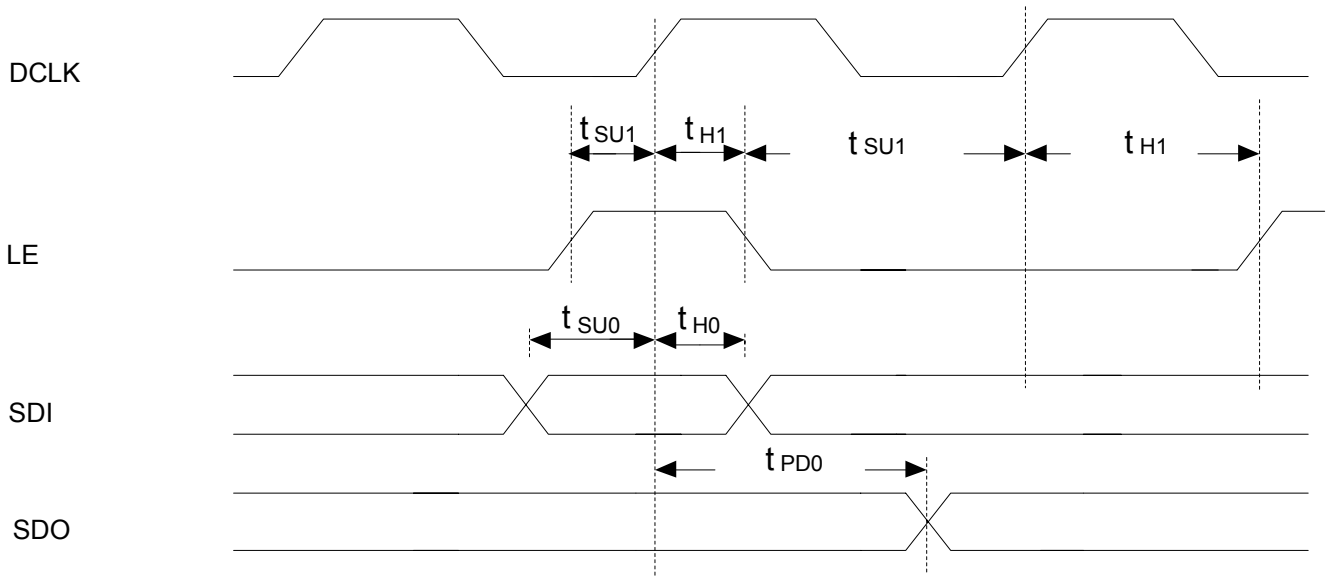


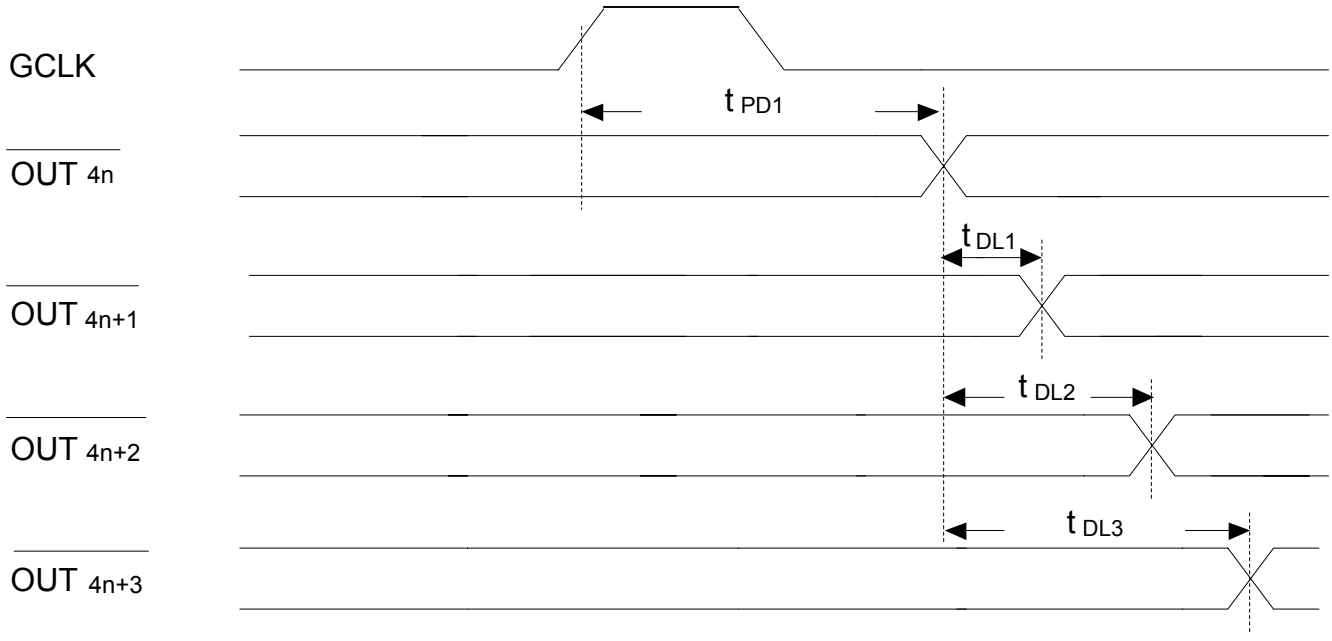
Figure 3

Timing Waveform

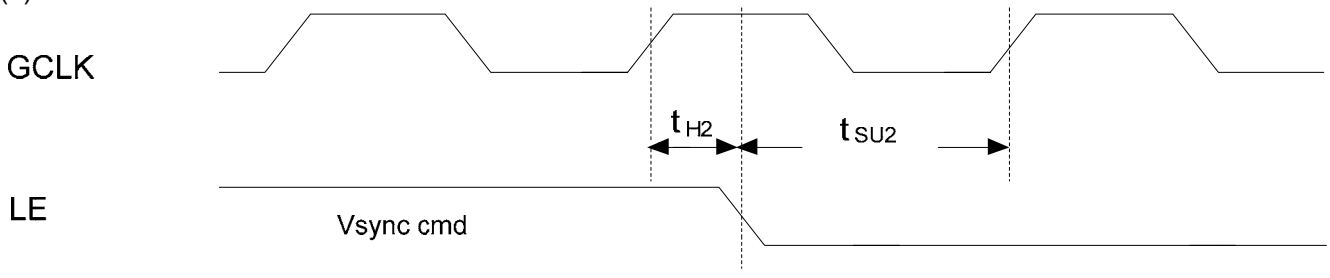
(1)



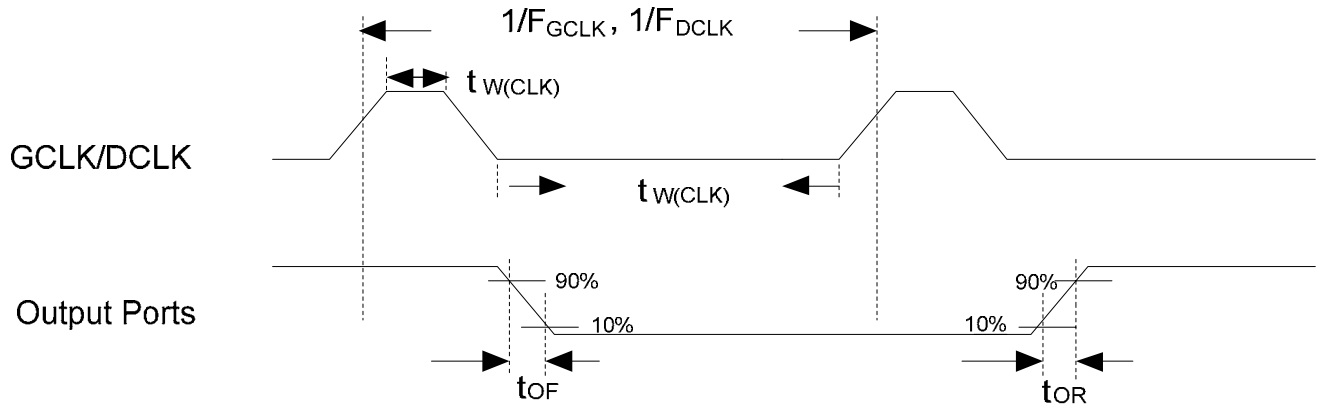
(2)



(3)



(4)


1/FGCLK，1/FDCLK
tW(CLK)
GCLK/DCLK
tW(CLK)
Output Ports
90%
10%
90%
10%
tOF
tOR

Control Command

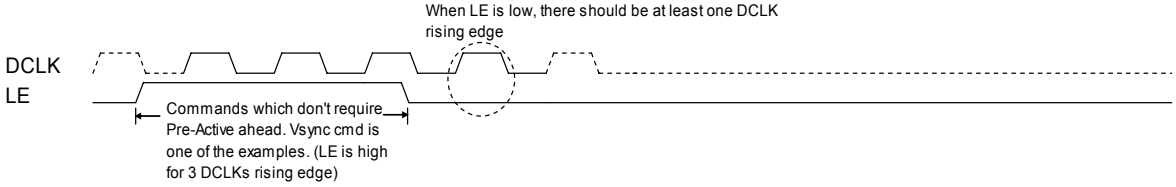
	Signals Combination		Description
Command Name	**LE**	**Number of DCLK Rising Edge when LE is asserted**	**Action of Command**
Data Latch	High	1	Serial data are transferred to the input data buffers
Vsync	High	3	Vertical Synchronal signal. Display frame will be updated to output channel
Write Configuration*	High	4	Serial data are written to the configuration register
Read Configuration	High	5	Serial data are read from the configuration register
Software Reset	High	10	Reset the behavior of MBI5050 except the configuration registers value
Pre-Active	High	14	Pre-Active command needs to be sent before “Write Configuration” command.

*Those commands can only be activated after Pre-Active command; otherwise, they will be invalid.

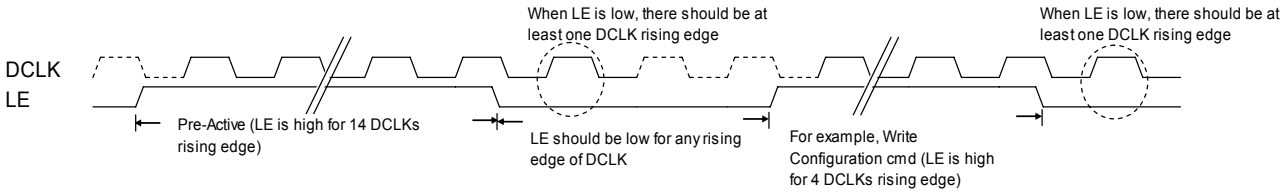
Note: When the power is on, Vsync command will be valid only after 16 times of “Data Latch” commands have been sent in advance.

The following figures show the waveforms of commands which require or don’t require “Pre-Active” ahead.

Commands which don't require Pre-Active ahead



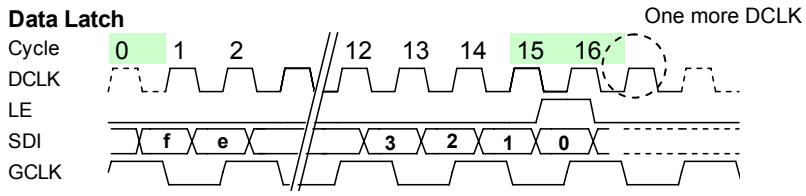
Commands which require Pre-Active ahead



Waveform of Commands

The following figures show the waveform of each command. For every command, there must be at least one more DCLK after LE goes low.

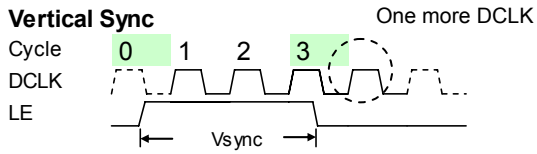
Data Latch



Data Latch command is used to latch the 16-bit shift register from SDI to internal SRAM buffer. When this command is received, the last 16 bits data before the falling edge of LE will be latched into SRAM, as shown in the above waveform, and MSB bit needs to be sent first.

Note: GCLK cannot stop during this command. Ratio of GCLK frequency to DCLK frequency should be ≧20%.

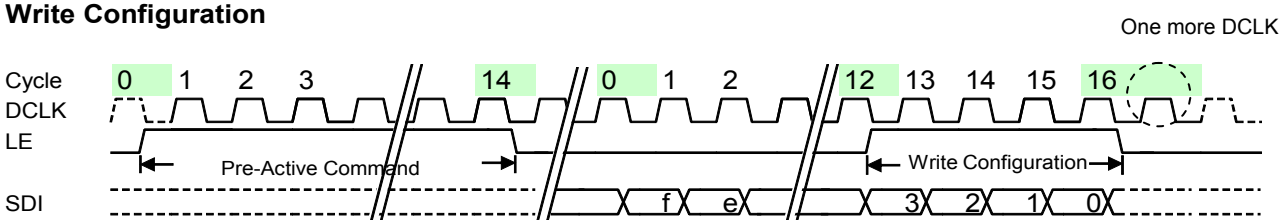
Vertical Sync



"Vsync" command is used to update frame data on output channels (OUT0~OUT15). There are some timing limitations between signal "LE" and "GCLK"; and please refer to the section of "Vsync Command Operation" for details.

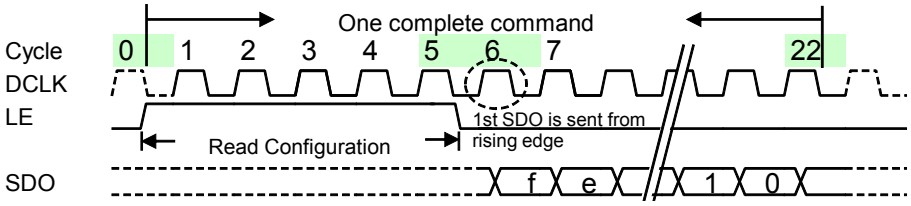
Note: The extra DCLK after LE goes low is required for GCLK≠DCLK mode. Please refer to "Vsync Command Operation" for detailed information.

Write Configuration



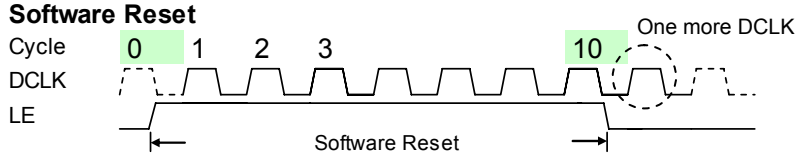
"Write configuration" command is used to program the configuration register of MBI5050. The "Pre-Active" command must be sent in advance. When this command is received, the last 16 bits data before the falling edge of LE will be latched into configuration register, as shown in the above waveform, and MSB bit needs to be sent first.

Read Configuration



"Read configuration" command is used to read the configuration register of MBI5050. When this command is received, the 16-bit data of configuration register will be shifted out from SDO pin, as shown in the above waveform, and MSB bit will be shifted out first.

Software Reset



“Software reset” command makes MBI5050 go back to the initial state except configuration register value. After this command is received, the output channels will be turned off and will display again with last gray-scale value after new “Vsync” command is received.

Definition of Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	6’b101011					

Default setting of configuration register is 16’h032B

Bit	Attribute	Definition	Value	Function
F	Read/Write	Reserved	0 (Default)	Reserved. Please set “0”.
E	Read/Write	Reserved	0 (Default)	Reserved. Please set “0”.
D	Read/Write	GCLK source	0 (Default)	GCLK sent by user
			1	Set GCLK=DCLK. Use DCLK to be the source of GCLK.
C	Read/Write	Gray scale mode	0 (Default)	16-bit Gray scale mode. The 65,536 GCLKs (16-bit) PWM cycle is divided into 64 sections. Each section has 1,024 GCLKs.
			1	14-bit Gray scale mode. The 16,384 GCLKs (14-bit) PWM cycle is divided into 16 sections. Each section has 1,024 GCLKs. User should still send 16-bit data with 2-bit 0 in LSB bits. e.g. {14’h1234, 2’h0}.
B	Read/Write	Reserved	0 (Default)	Reserved. Please set “0”.
A~8	Read/Write	Number of scan lines	000 001 010 011 (Default) ~ 111	000: 1 scan line 001: 2 scan lines 010: 3 scan lines 011: 4 scan lines 100: 5 scan lines 101: 6 scan lines 110: 7 scan lines 111: 8 scan lines
7~6	Read/Write	Reserved	00(Default)	Reserved. Please set “0”.
5~0	Read/Write	Current gain adjustment	000000~ 111111	6’b101011 (Default) Allow 64-step programmable current gain from 12.5 % to 200%

Number of Scan Line

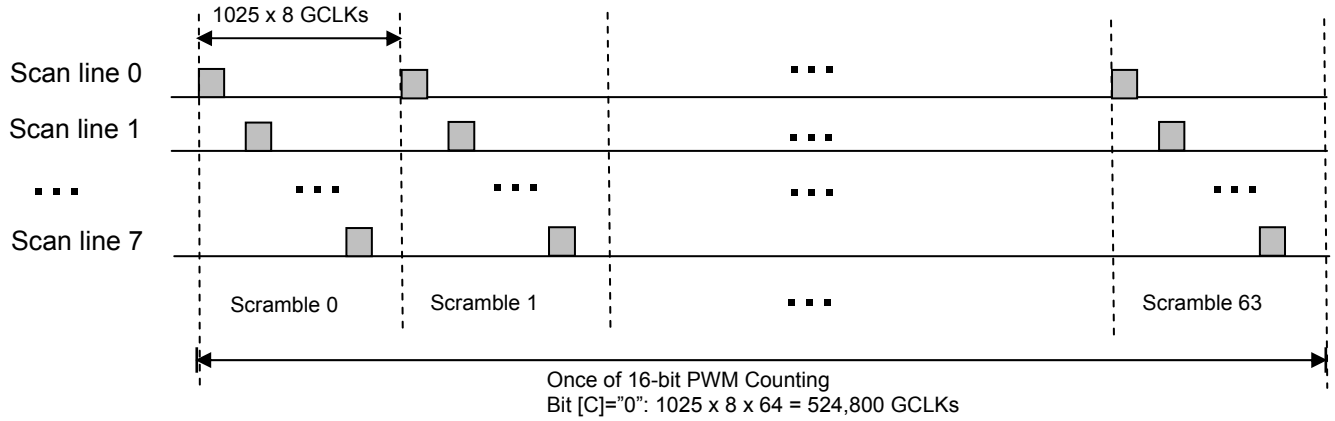
MBI5050 supports 1 to 8 scan lines. Please set the configuration register bit [A:8] according to the application. The default value '011' is 4 scan lines.

Gray Scale Mode and Scan-type S-PWM

MBI5050 provides a selectable 16-bit or 14-bit gray scale by setting the configuration register bit [C]. The default value is set to '0' for 16-bit color depth. In 14-bit gray scale mode, users should still send 16-bit data with 2-bit '0' in LSB bits. For example, {14'h1234, 2'h0}.

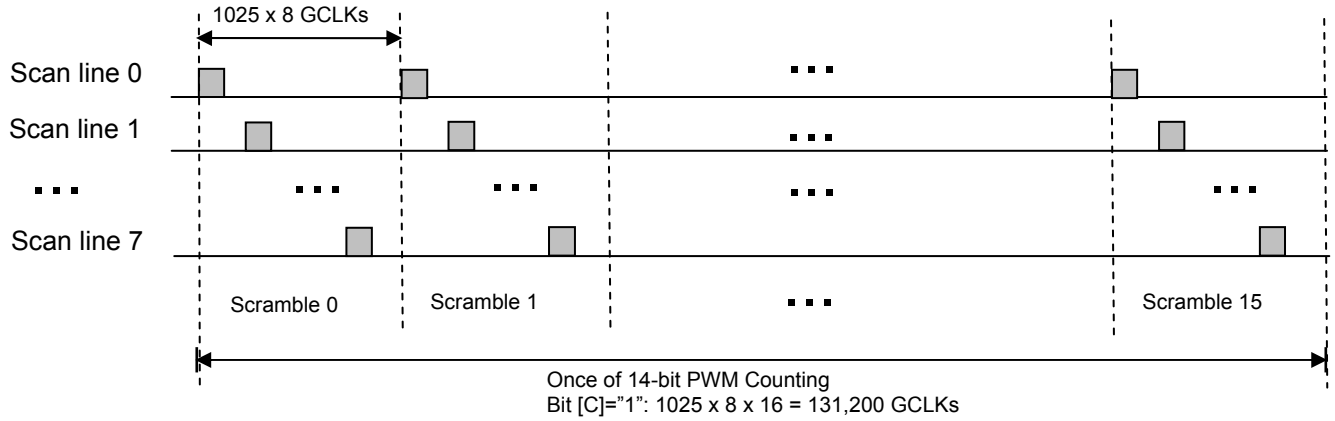
Configuration register bit [C] also decides the S-PWM mode for scan type. MBI5050 has a smart S-PWM technology for scan type. With S-PWM, the total PWM cycles can be broken into MSB (Most Significant Bits) and LSB (Least Significant Bits) of gray scale cycles. The MSB information can be broken down into many refresh cycles to achieve overall same high bit resolution.

Display sequence of 64 scrambles



: Output ports are turned "on".

Display sequence of 16 scrambles



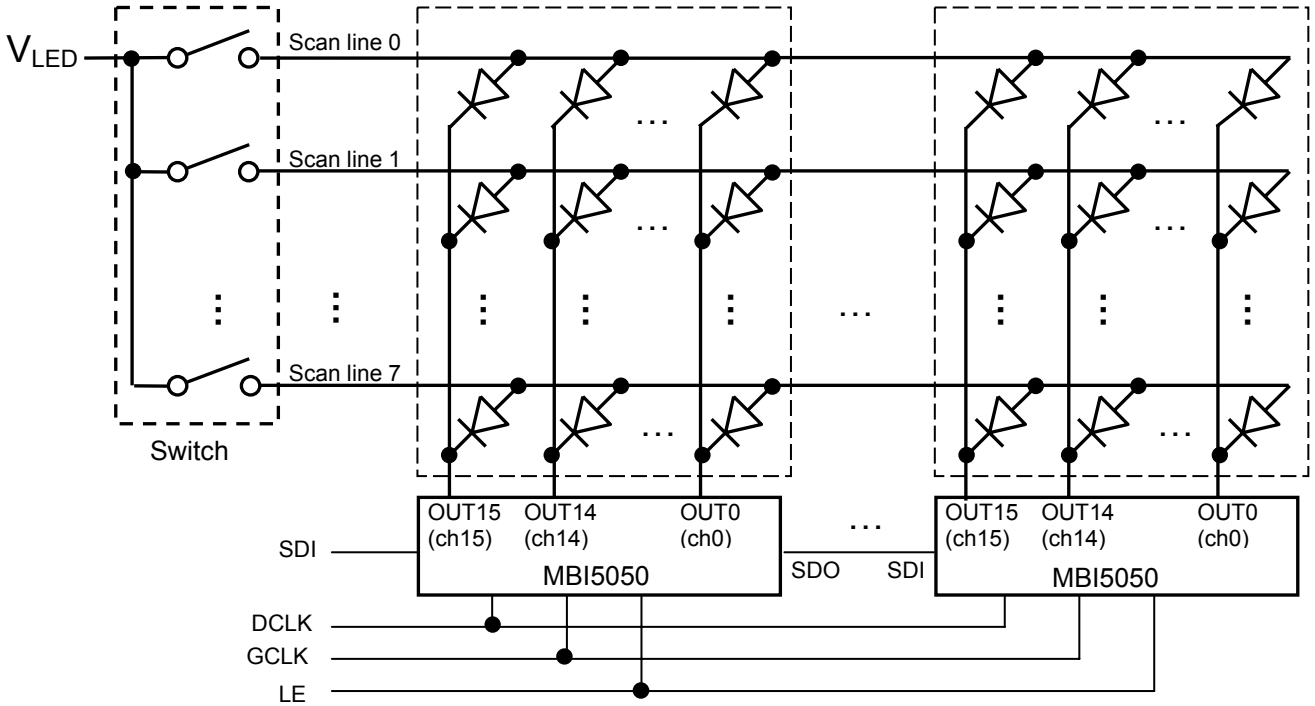
: Output ports are turned "on".

GCLK Source

Users could choose GCLK source by setting the configuration register bit [D]. The default value is '0' that GCLK is controlled by users. The GCLK tracing on PCB could be saved by choosing GCLK=DCLK.

Operation Principal

Scan type application structure



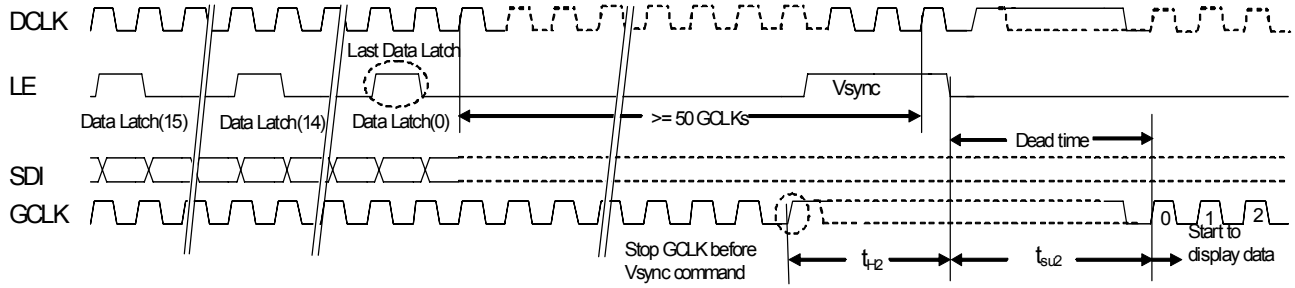
The above figure shows the suggested application structure of scan type scheme with 8 scan lines. The gray-scale data are sent by pin “SDI and SDO” with the commands formed by pin “LE” and “DCLK”. The output ports from 16 channels ($\overline{OUT0}$ ~ $\overline{OUT15}$) will output the PWM result for each scan line at different time, so there must be one “Switch” to multiplex for each scan line. The switching sequence and method and the command usage will be described in the following section.

Initialization Sequence

At initialization, users need to program the configuration register, if the default value of the register is not what they want. Then, the users need to send the gray scale data by the number of "Data Latch" commands (16 x number of scan lines), and then send one Vsync command to start to display.

For the initial sequence, users should only send Vsync command after 50 GCLKs of the last "Data Latch" command as shown in the below waveform. The display data will not start until first Vsync command is ready. The GCLK must be stopped before Vsync command is set, and there are some timing limitations which will be described in detail in the following section.

Start to display data for initial case

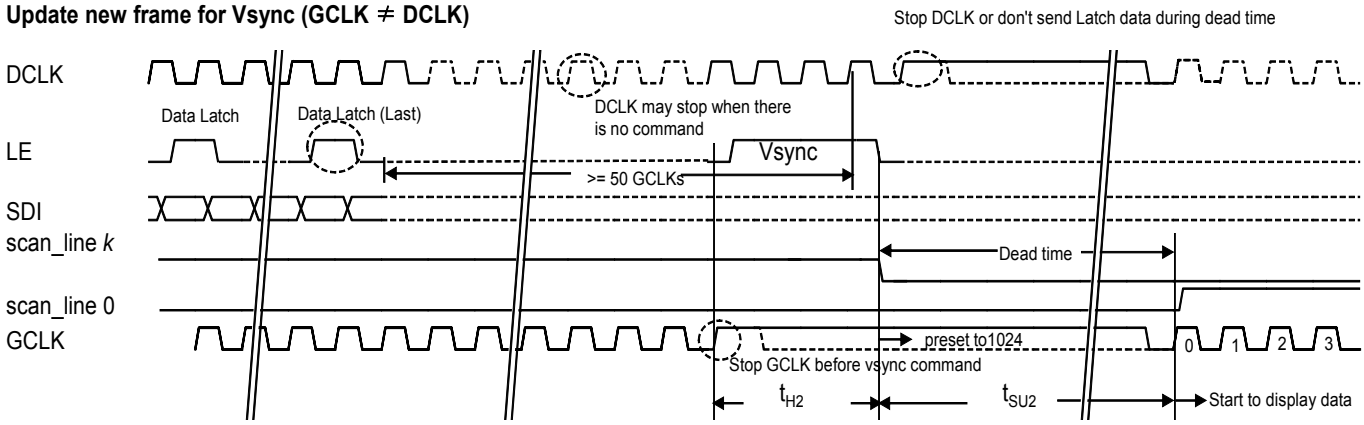


Vsync Command Operation

"Vsync" command is set when users want to update the image frame. Below waveforms show the Vsync command to update the frame, when GCLK is independent of or equal to DCLK.

If GCLK ≠ DCLK:

Update new frame for Vsync (GCLK ≠ DCLK)



There are limitations for users to follow:

a.) Since the gray scale data needs time to pre-read from SRAM to internal display buffer after last Data Latch command, there should be at least 50 GCLKs before the Vsync command is sent
Note: More details about SRAM memory structure can be referred to the section of Memory Structure.

b.) It is suggested for controller to keep one GCLK counter (from 0~1024), which will preset to 1024 at the falling edge of LE of Vsync command and restart from 0 at next GCLK.

c.) Since Vsync is the LE clock domain, there is a timing limitation between LE and GCLK. The GCLK should stop before Vsync command is sent. The setup and hold time between LE's falling edge and GCLK's rising edge must meet the t_{SU2} and t_{H2}, respectively.

d.) The GCLK also needs to stop for dead time. The dead time is the time interval between scan lines, and is controlled by stopping GCLK. When Vsync command is set, the frame will be updated. The scan line needs to be switched (by controller) from scan line *k* to scan line 0, too.

e.) DCLK can either stop or not when there is no command.

f.) During dead time, user needs to either stop DCLK or cannot send “Data Latch” command.

g.) The new data will be loaded to internal display buffer at Vsync command. But it will start to display after dead time is finished.

If GCLK = DCLK

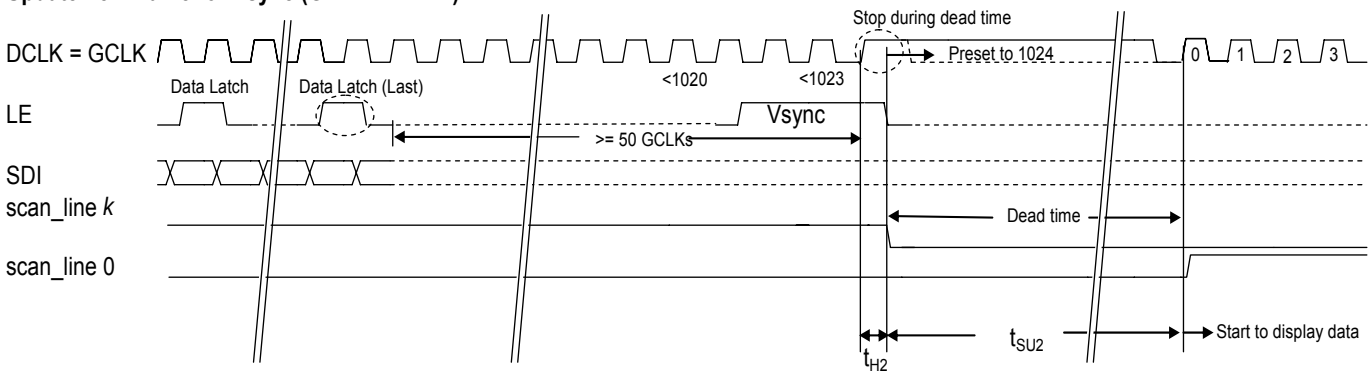
The control behavior is a little different from above:

a.) The DCLK cannot stop after finishing sending command due to DCLK also acts as GCLK.

b.) The DCLK needs to stop after finishing sending Vsync command for dead time. Of course, the setup and hold time between LE's falling edge and GCLK's rising edge must meet the t_{SU2} and t_{H2}, too.

c.) The stop point of DCLK for Vsync command can only be set before GCLK counter is < 1023.

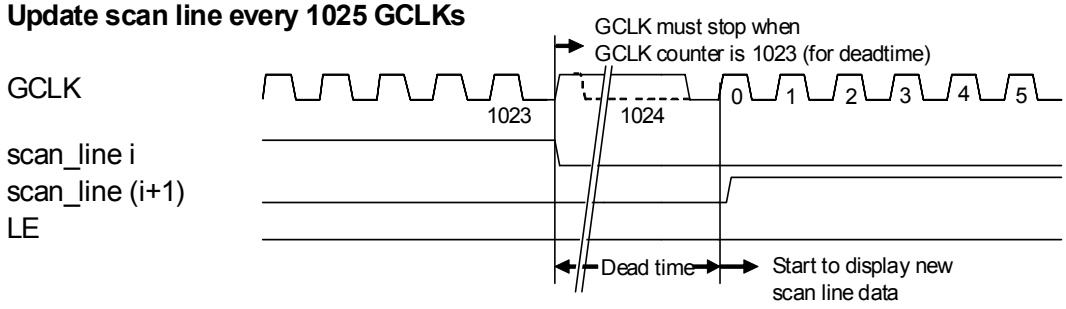
Update new frame for Vsync (GCLK = DCLK)



Switch Scan Line Inside Each Frame

For the control of scan line switch, users should count in the same way of MBI5050's GCLK counter and switch each scan line when MBI5050 GCLK counter counts to 1023, and please refer to the section of Gray Scale Mode and Scan-type S-PWM for the multiplexing sequence. The dead time is controlled by stopping GCLK. MBI5050 will turn off output channels when GCLK counter value equals to 1024 during dead time.

Update scan line every 1025 GCLKs



Summary

The control sequence is described as below:

1. Users program the configuration register by "Write Configuration" command.
2. Users send gray scale data by the number of "Data Latch" commands (16 x number of scan lines).
3. After last "Data Latch" command, users must wait for more than 50 GCLKs before sending Vsync command. If it is not the first frame, users should send Vsync command according to the frame rate. For example, if the frame rate is 60, users should wait for 1/60 seconds. When users send Vsync command, the related timing limitations must be followed.
4. When users send Vsync command, the scan line needs to start to count from 0. GCLK counter needs to be pre-set to 1024 and stops GCLK for dead time.
5. During the frame display period, users need to keep one GCLK counter (0~1024) and switch scan line and insert dead time (by stopping GCLK) when GCLK counter counts to 1023.

6. During dead time (for both sending Vsync command or when GCLK counter equals to 1024), it's not allowed to send "Data Latch" command.
7. The gray scale data of the next frame may be sent after Vsync command is sent.
8. It's strongly recommend that "Write Configuration" command should be sent periodically to avoid system noise interference.

Visual Refresh Rate

In 16-bit S-PWM mode, the visual refresh rate will be improved by 64x, if the data is ≧64.
In 14-bit S-PWM mode, the visual refresh rate will be improved by 16x, if the data is ≧16.

The formula of visual refresh rate is:
Visual refresh rate = GCLK frequency / [(1024 GCLK + dead time) x number of scan lines]

For example, if there are 4 scan lines with 16-bit scan-type S-PWM, the GCLK frequency is 10MHz. The dead time is 10 GCLK periods. Then the visual refresh rate could be calculated as below:
Visual refresh rate = 10MHz / [(1024+10) x 4] = 2418Hz.

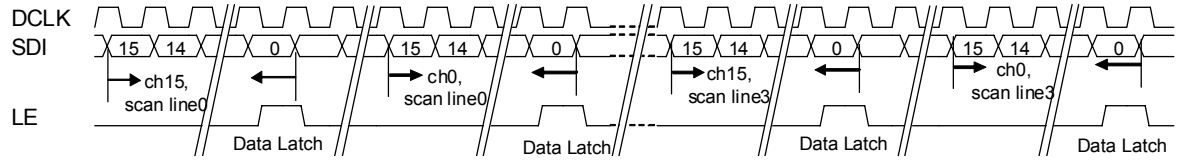
Data Input Sequence

The sequence of input data starts from scan line 0 first, then scan line 1, and so on.
During each scan line, gray-scale data of channel 15 needs to be sent first, and then channel 14, continuously to channel 0.
Please refer to the section of scan type application structure for scan type scheme.
The following examples are the waveforms with 1 LED driver and 2 cascaded LED drivers respectively.

1x IC, 4 scan lines

For only one LED driver used, there are 16 bits for each channel, and note that MSB bit is sent first.

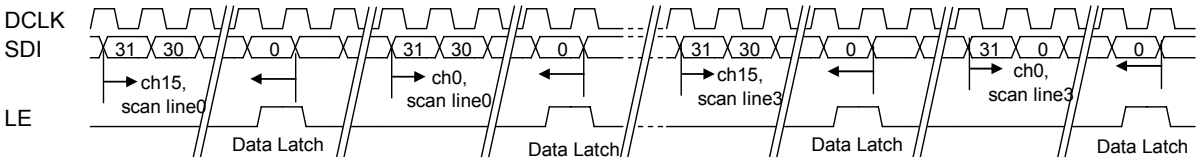
1xIC, 4 scan lines



2x ICs, 4 scan lines

For two LED drivers cascaded, there are 16 bits for each LED driver, so there are 32 bits for each channels, first 16 bits (bit31 ~ bit16) is for 2nd LED driver, and last 16 bits (bit15 ~ bit0) is for 1st LED driver, note that MSB bit is sent first, too.

2xICs, 4 scan lines

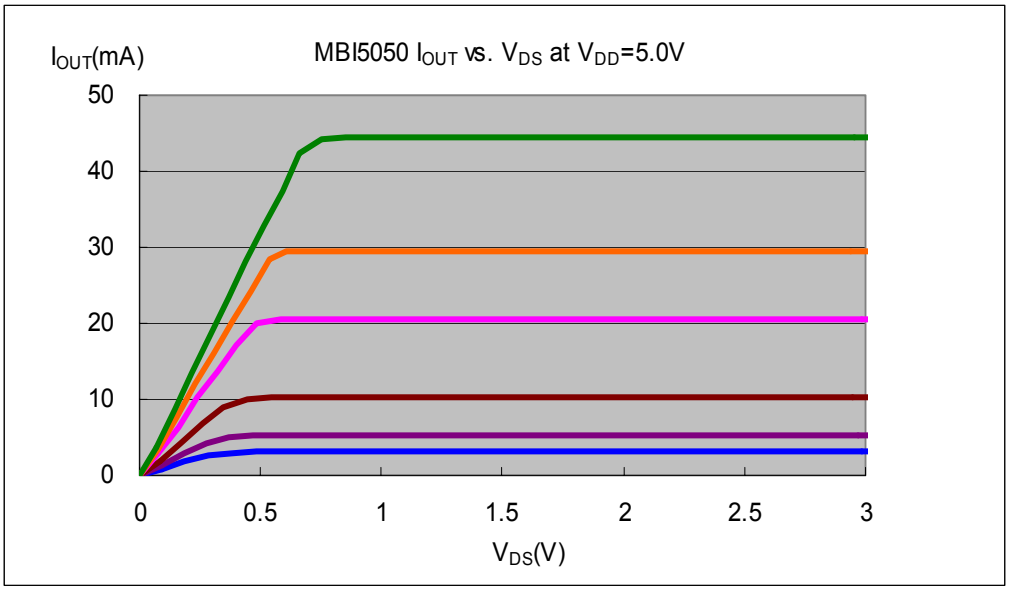


Constant Current

In LED display application, MBI5050 provides nearly no variation in current from channel to channel and from IC to IC. This can be achieved by:

1) The typical current variation between channels is less than 1.5%, and that between ICs is less than ±3%.

2) In addition, the current characteristic of output stage is flat and user can refer to the figure below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This guarantees LED to be performed on the same brightness as user's specification.



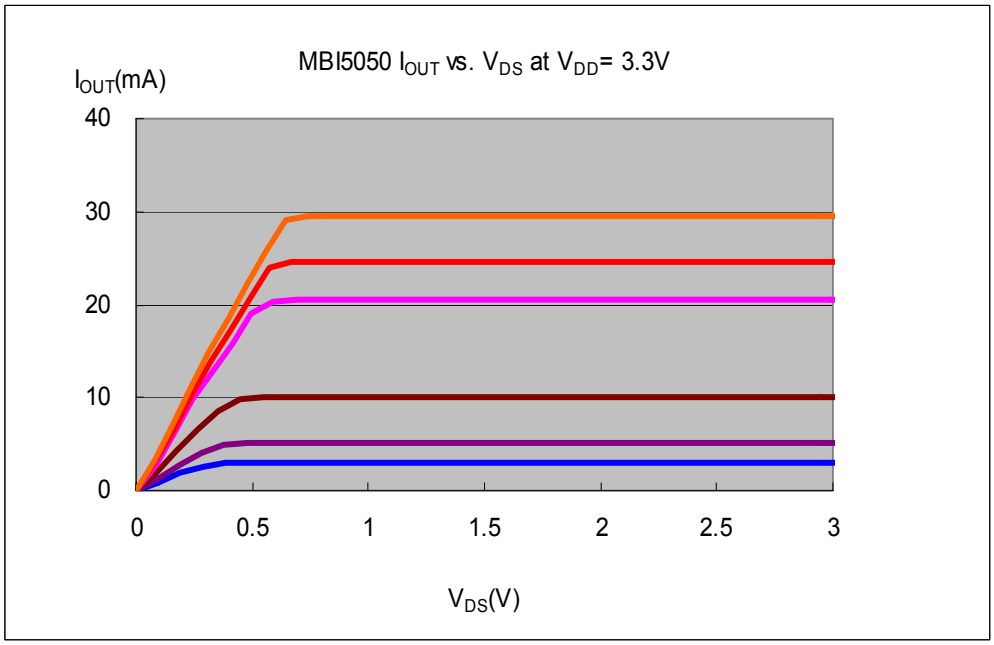
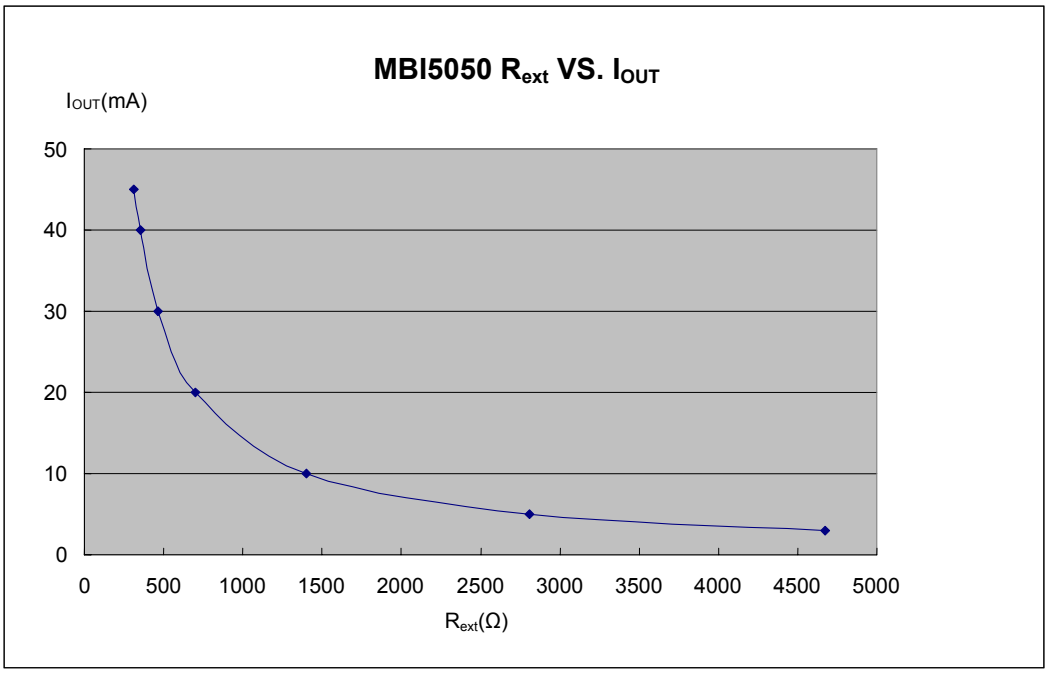


Figure 4

Setting Output Current

The output current (I_{OUT}) is set by an external resistor, R_{ext}. The default relationship between I_{OUT} and R_{ext} is shown in the following figure.



Also, the output current can be calculated from the equation:

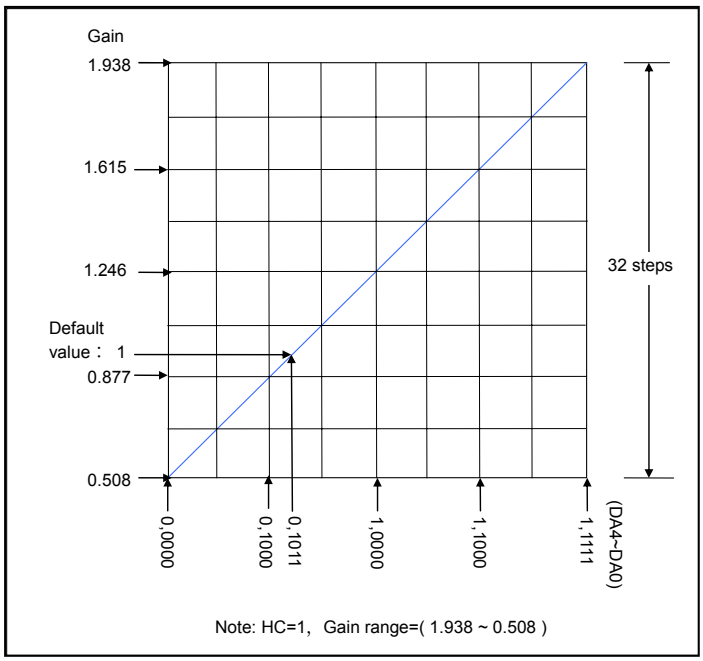
$V_{R\text{-}EXT}$=0.61Volt x G x H; $I_{OUT}=V_{R\text{-}EXT}/(R_{ext}$ x H)x25.0

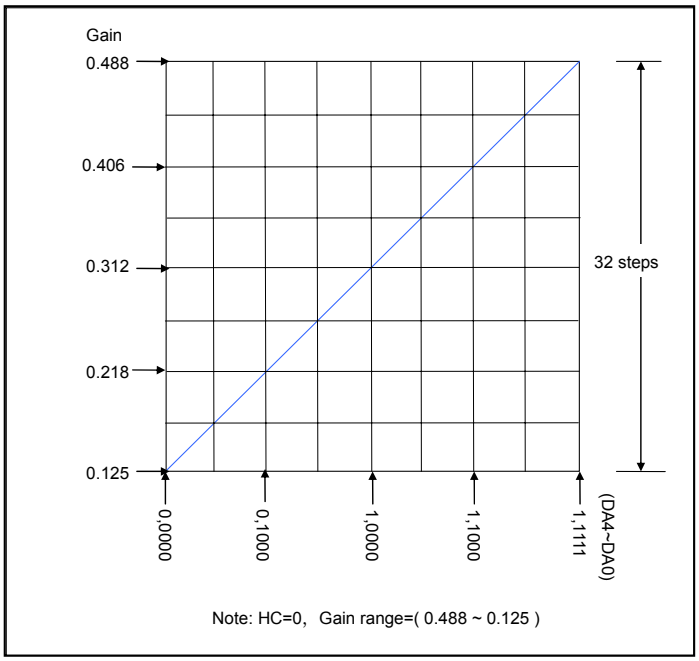
HC=1=>H=1 (Please refers to Current Gain Adjustment section for “HC” description)

HC=0=>H=4

Whereas R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is its voltage. G is the digital current gain, which is set by the bit 5 ~ bit 0 of the configuration register. The default value of G is 1. For your information, the output current is about 22.4mA when R_{ext}=680Ω if G is set to default value 1. The formula and setting for G are described in next section.

Current Gain Adjustment





The 6 bits (bit 5~bit 0) of the configuration register set the gain of output current, i.e., G. As total 6-bit in number, i.e., ranging from 6'b000000 to 6'b111111, these bits allow user to set the output current gain up to 64 levels. These bits can be further defined inside configuration register as follows:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	HC	DA4	DA3	DA2	DA1	DA0

1. Bit 5 is HC bit. The setting is in low current band when HC=0, and in high current band when HC=1.
2. Bit 4 to bit 0 are DA4 ~ DA0.

The relationship between these bits and current gain G is:

HC=1, D=(65xG-33)/3

HC=0, D=(256xG-32)/3

and D in the above decimal numeration can be converted to its equivalent in binary form by the following equation:

$D= DA4x2^4+DA3x2^3+DA2x2^2+DA1x2^1+DA0x2^0$

In other words, these bits can be looked as a floating number with 1-bit exponent HC and 5-bit mantissa DA4~DA0.

For example,

HC=1, G=1.246, D=(65x1.246-33)/3=16

the D in binary form would be:

$D=16=1x2^4+0x2^3+0x2^2+0x2^1+0x2^0$

The 6 bits (bit 5~bit 0) of the configuration register are set to 6'b110000.

Staggered Delay of Output

MBI5050 has a built-in staggered circuit to perform delay mechanism. Among output ports exist a incremental 5ns delay time among $\overline{OUT4n}$, $\overline{OUT4n+1}$, $\overline{OUT4n+2}$, and $\overline{OUT4n+3}$, by which the output ports will be divided to four groups at a different time so that the instant current from the power line will be lowered.

Package Power Dissipation (PD)

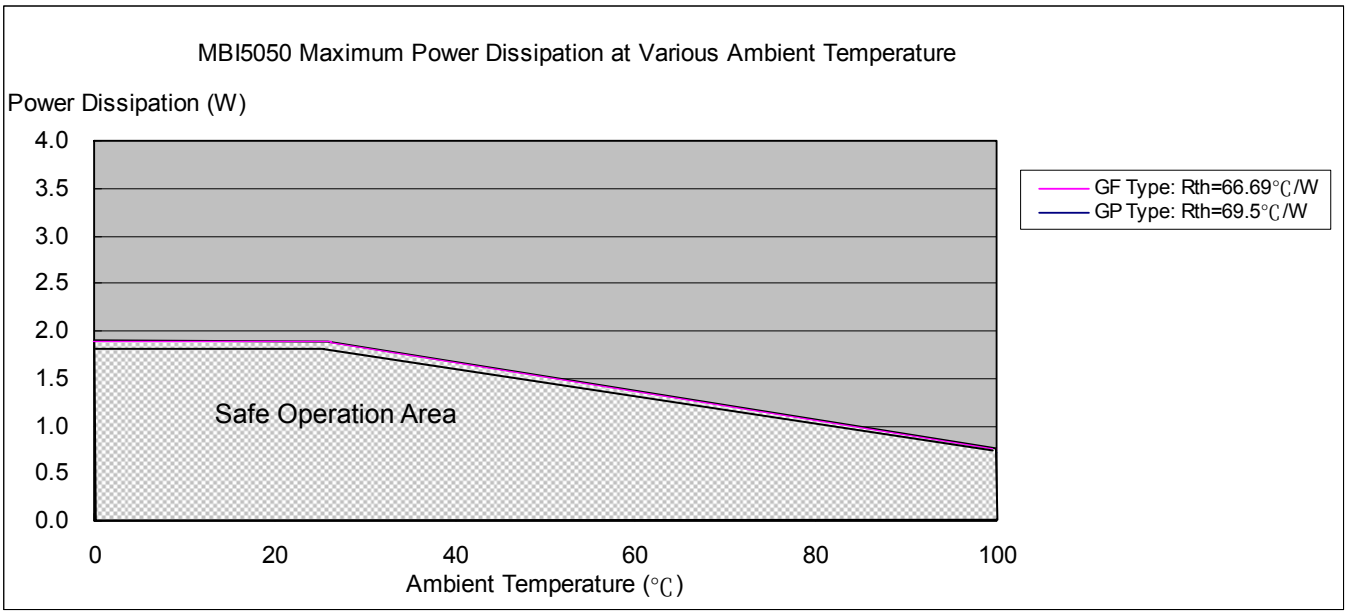
The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep $P_D(act)\leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/16$, where Tj=150°C.

Please see the follow table for P_D and $R_{th(j-a)}$ for different packages:

Device Type	$R_{th(j-a)}$ (°C/W)	P_D (W)
GF	66.69	1.87
GP	69.5	1.79

The maximum power dissipation, $P_D(max)=(Tj–Ta)/R_{th(j-a)}$, decreases as the ambient temperature increases.



LED Supply Voltage (V_{LED})

MBI5050 is designed to operate with V_{DS} ranging from 0.4V to 1.0V (depending on I_{OUT}=3~45 mA) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D\ (act)} > P_{D\ (max)}$ when V_{LED}=5V and $V_{DS}=V_{LED}-V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

A voltage reducer lets $V_{DS}=(V_{LED}-V_F)-V_{DROP}$.

Resistors or Zener diode can be used in the applications as shown in the following figures.

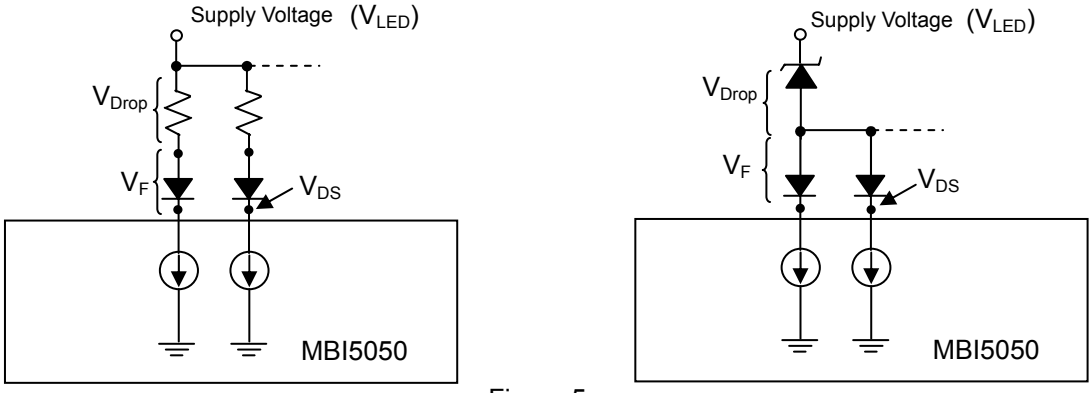


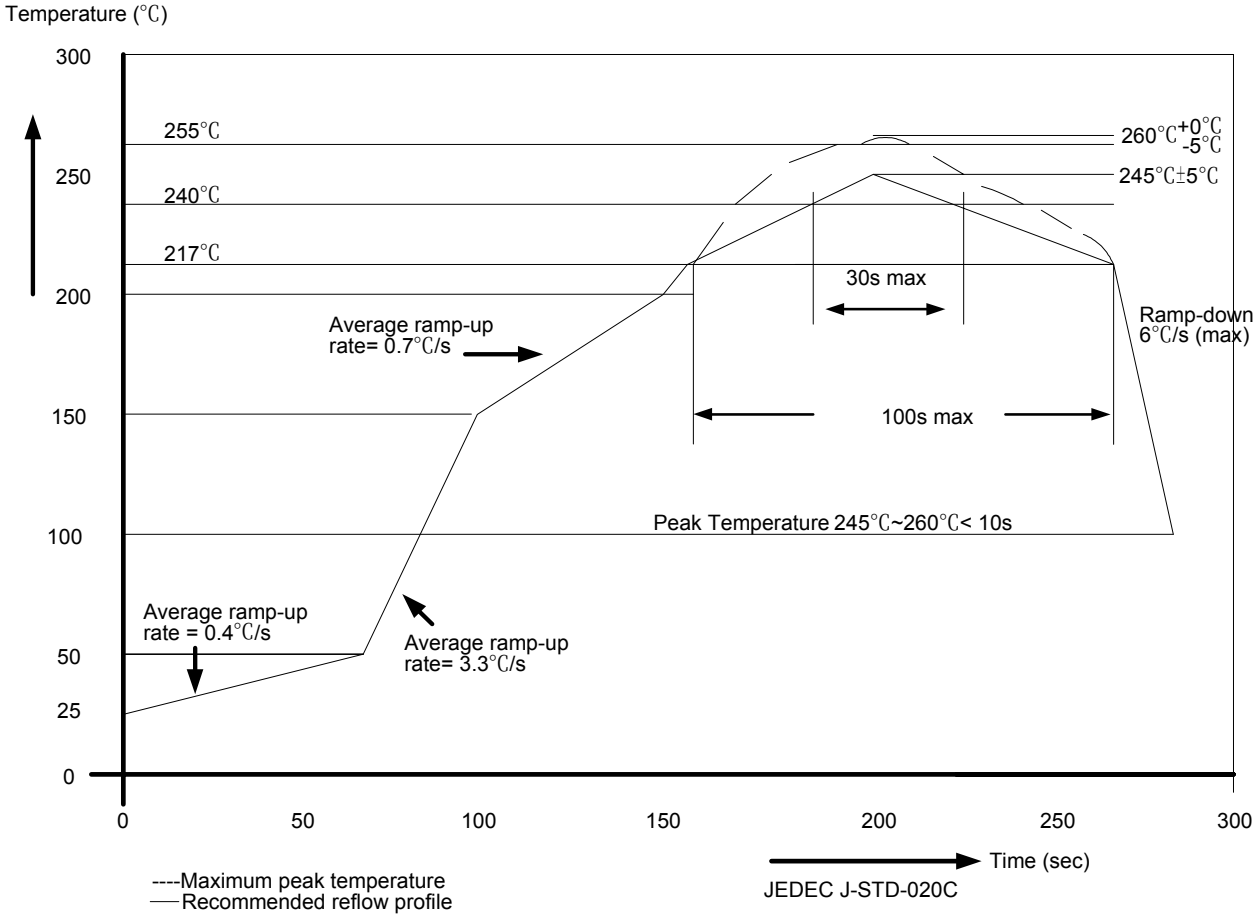
Figure 5

Switching Noise Reduction

LED drivers are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers- Overshoot”.

Soldering Process of "Pb-free" Package Plating*

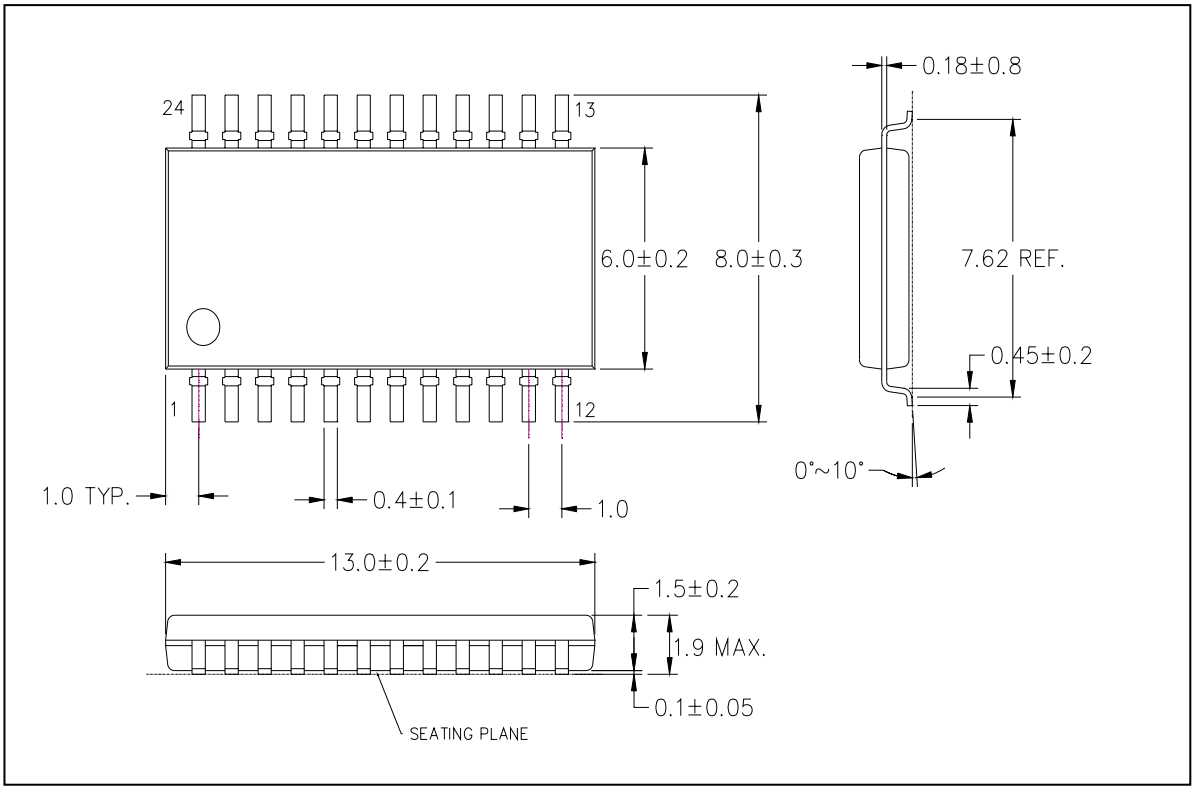
Macroblock has defined "Pb-Free" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it adopts tin/lead (SnPb) solder paste, and please refer to the JEDEC J-STD-020C for the temperature of solder bath. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below. .



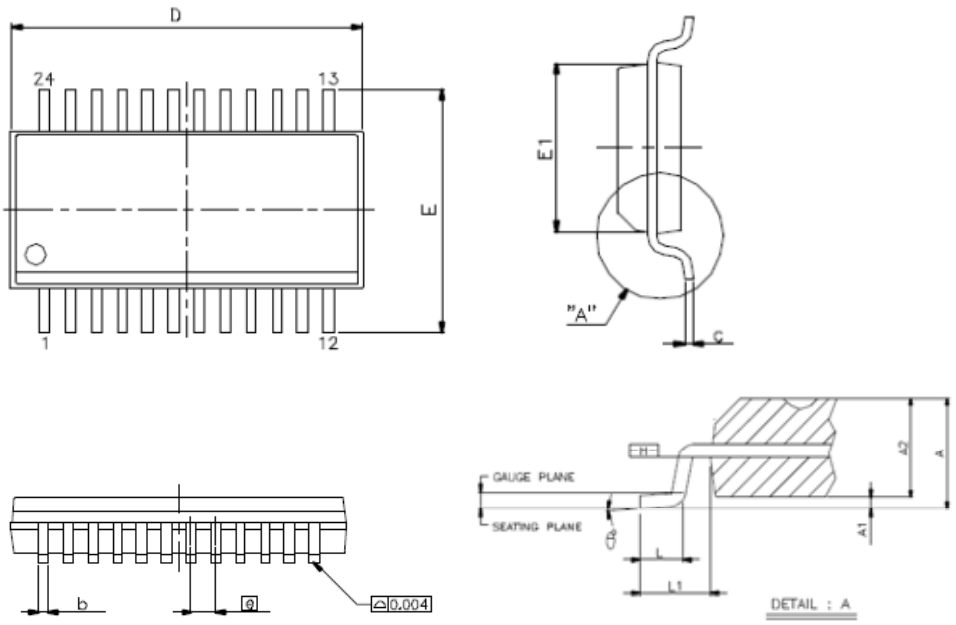
Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

*Note: For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Outline



MBI5050 GF Outline Drawing

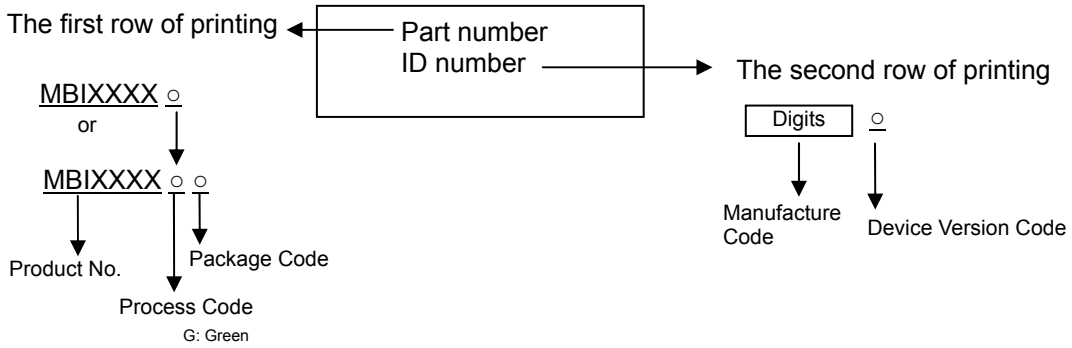


SYMBOLS	Dimensions shown in inchs			Dimensions shown in millimeters		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.053	0.064	0.069	1.346	1.626	1.753
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	—	—	0.059	—	—	1.499
D	0.337	0.341	0.344	8.560	8.661	8.738
E	0.228	0.236	0.244	5.791	5.994	6.198
E1	0.150	0.154	0.157	3.810	3.912	3.988
b	0.008	—	0.012	0.203	—	0.305
c	0.007	—	0.010	0.178	—	0.254
L	0.016	0.025	0.050	0.406	0.635	1.270
e	0.025 BASIC			0.635 BASIC		
L1	0.041 BASIC			1.0414 BASIC		
θ°	0	—	8	0	—	8

MBI5050 GP Outline Drawing

Note: The unit for the outline drawing is mm.

Product Top Mark Information



Product Revision History

Datasheet version	Device Version Code
V1.00	A
V1.01	A
V1.02	A
V1.03	A

Product Ordering Information

Part Number	"Pb-free & Green" Package Type	Weight (g)
MBI5050GF	SOP24-236-1.00	0.28
MBI5050GP	SSOP24-150-0.64	0.11

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